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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention is ** about a semiconductor memory device and a manufacturing method for the same, and relates to a semiconductor memory device which uses a high dielectric (high dielectric) as a capacitor dielectric film in more detail, and a manufacturing method for the same.
[0002]
[Description of the Prior Art]The minimum line width for embodying dynamic RAM products these days is rapidly reduced below by a quarter micrometer (0.25 micrometer). When a stack type cell capacitor storage electrode (stacked-type cell capacitor storage electrode) is formed in the same flat surface, the layout (layout) of said storage electrode -- dynamic RAM cell area -- extensive -- rather than a layout area, it depends for the usable area of a storage electrode on the lateral area of a storage electrode heavily by rare one which is.
[0003]however, Since thickness expansion of a storage electrode spreads the surface step of a dynamic RAM cell and a periphery (periphery) and makes metallic wiring (metal interconnection) difficult by a following process. There is a limit in thickness expansion of a storage electrode by a stack type dynamic RAM cell. Therefore, since cell area reduction paraphrasing **** by high integration and a surface step are contracted, usable area reduction of a cell capacitor storage electrode is in an unavoidable situation.
[0004]On the other hand, voltage lowering of the latest dynamic RAM is carried out, and since the data sensing (data sensing) method by voltage difference is maintained and continues, the capacitor capacity of a dynamic RAM cell needs 25-30fF. Therefore, it is concentrated on increasing the dielectric constant of a cell capacitor dielectric for high integration of a dynamic RAM.
[0005]Although they are used in the conventional cell capacitor, making capacitor dielectric films, such as a silicon nitride (Si_3N_4) and tantalum oxide (Ta_2O_5), laminate on a storage electrode, As for the dielectric film of a cell capacitor, practical use of 10000 or more substances is known for bulk (bulk) dielectric constants, such as strontium titanate ($SrTiO_3$) or barium titanate strontium (Ba, Sr) (TiO_3), by high integration of the element.
[0006]Since a capacitor high dielectric builds a low dielectric film (SiO_2) to the interface of polysilicon and the leak current of a dielectric film is made to increase when using a polysilicon film as a storage electrode, a problem is generated at the time of application of a product.

[0007]Therefore, since it is hard to use such a new dielectric film with the existing polysilicon electrode, a new electrode and electrode structure are required. Transition metals (transition metal), such as platinum (Pt), iridium (Ir), and a ruthenium (Ru), are among the substances well known as an electrode for BST now. Since a transition metal is stabilized chemically and does not oxidize, even if it passes through a high temperature process required for a BST formation process, it does not form a low dielectric layer in an interface with BST.
[0008]Drawing 1 (A) and drawing 1 (B) are the figures showing the conventional semiconductor memory device and the process of the manufacturing method one by one. As for reference of drawing 1 (A), a conventional semiconductor memory device and a manufacturing method for the same will form the gate electrode layer 13 on the semiconductor substrate 10 first. The oxide film 14 is formed with an insulator layer on the semiconductor substrate 10 including the gate electrode layer 13. Bit lines are formed in the oxide film 14 (not shown).
[0009]The storage electrode contact hole 16 is formed by etching the oxide film 14 until the surface of the semiconductor substrate 10 is exposed using the mask for contact hole formation. The storage electrode contact plug 17 which conductive material like polysilicon is filled up with the contact hole 16, and is electrically connected with the semiconductor substrate 10 is formed.
[0010]The barrier film 18 is formed on the oxide film 14 including the plug 17. The oxide in which the barrier film 18 contains at least one in barium (Ba), strontium (Sr), and a ruthenium (Ru), TiN, TiSiN, TiAlN, TaSiN, TaAlN, ruthenium oxide (RuO_2), It is formed by any one in iridium oxide (IrO_2) and lanthanum trioxide strontium cobalt (LSCO). The barrier film 18 is thinly formed by a thickness of 500 A.
[0011]Here, the barrier film 18 is a film for preventing polysilicon of the morphogenetic substance of the plug 17 from oxidizing. The conducting film 20 for storage electrodes is formed on the barrier film 18. The conducting film 20 is formed by any one in barium, strontium, the oxide that contains at least one in a ruthenium, a ruthenium and platinum, iridium, iridium oxide, ruthenium oxide, and lanthanum trioxide strontium cobalt. The conducting film 20 is thickly formed in [thickness] 2000A thru/or 4000 A.
[0012]A storage electrode layer is formed by etching the conducting film 20 and the barrier film 18 one by one using the mask 22 for storage electrode formation.
[0013]On the other hand, an oxide film is formed with an insulator layer on the conducting film 20 (not shown). A wrap spacer is thoroughly formed in each side walls of the barrier film 18 by carrying out overall etching of the insulator layer at an etchback (etch back) process (not shown). A spacer is used as a film for preventing oxidation of the barrier film 18 by a following process at the time of formation of a high dielectric film, when the barrier film 18 is formed by the substance which the silicon component contained.
[0014]Then, the capacitor dielectric film 24 is formed on the conducting film 20 (drawing 1 (B)). The capacitor dielectric film 24 is formed with any one high dielectric film in strontium titanate ($SrTiO_3$) and barium titanate strontium (Ba, Sr) (TiO_3). A capacitor is formed by forming the upper electrode 26 of a capacitor on the capacitor dielectric film 24.
[0015]A layout area may be made to reduce as a capacitor formed by a method which was mentioned above. However, since etching by-product generation of the time volatility of reactive ion etching is difficult for a transition metal in the field where the pattern whose interval of a storage electrode is about 0.1 - 0.2 micrometer at the time of the dry etching for storage electrode formation is dense, it is again vapor-deposited by the lower surface of the storage electrode side. Therefore, when the etching section of a storage electrode inclines toward the bottom side from the upper part, an interval with a storage electrode becomes narrow notably at bottom and the

thickness of a storage electrode becomes thick, the problem which the bridge (bridge) generates among these electrodes arises.
[0016]
[Problem(s) to be Solved by the Invention]The purpose of this invention is to provide a semiconductor memory device which can prevent the bridge between storage electrodes, and a manufacturing method for the same, maintaining the dry etching of the transition metal for storage electrode formation as it is.
[0017]
[Means for Solving the Problem]According to this invention for attaining the purpose mentioned above, a manufacturing method of a semiconductor memory device is provided with the following.
A stage which forms an insulator layer on a semiconductor substrate on which a transistor was accumulated.
A stage which etches an insulator layer and forms a contact hole until the surface of a semiconductor substrate is exposed using a mask for contact hole formation.
A stage which forms a plug which fills up a contact hole with conductive material and is electrically connected with a semiconductor substrate.
A stage which forms the 1st barrier film on an insulator layer including a plug, and a stage which forms the 1st conducting film for storage electrodes on the 1st barrier film, A stage which forms the 2nd barrier film on the 1st conducting film for storage electrodes, and a stage which forms the 2nd conducting film for storage electrodes on the 2nd barrier film, and forms the 2nd conducting film thinly relatively from the 1st conducting film, using a mask for storage electrode formation -- the 2nd conducting film, the 2nd barrier film, and the 1st conducting film -- and, A stage which forms a storage electrode layer which etches the 1st barrier film one by one, and is electrically connected with a plug, A stage which forms a barrier-metal spacer in each side walls of the 2nd conducting film, the 2nd barrier film, the 1st conducting film, and the 1st barrier film, and a stage which forms a conducting film spacer for storage electrodes in each side walls of a barrier-metal spacer.

[0018]According to this invention for attaining the purpose mentioned above, a semiconductor memory device is provided with the following.
Semiconductor substrate.
An insulator layer formed on a semiconductor substrate.
A plug which pierced through an insulator layer and was electrically connected with a semiconductor substrate.
A plug, the 1st barrier film formed on an insulator layer, and the 1st conducting film for storage electrodes formed on the 1st barrier film, A barrier-metal spacer formed in each side walls of the 2nd barrier film formed on the 1st conducting film, the 2nd conducting film thinly formed on the 2nd barrier film, the 2nd conducting film and the 2nd barrier film, the 1st conducting film, and the 1st barrier film, and a conducting film spacer formed in each side walls of a barrier-metal spacer.

[0019]According to this invention for attaining the purpose mentioned above, a manufacturing method of a semiconductor memory device is provided with the following.
A stage which forms an insulator layer on a semiconductor substrate on which a transistor was accumulated.

A stage which etches an insulator layer and forms a contact hole until the surface of a semiconductor substrate is exposed using a mask for contact hole formation.
A stage which forms a plug which fills up a contact hole with conductive material and is electrically connected with a semiconductor substrate.
A stage which forms a barrier film thickly on an insulator layer including a plug, and a stage which forms a conducting film for storage electrodes on a barrier film, and forms a conducting film thinly relatively from a barrier film, A stage which forms a storage electrode layer which etches a conducting film and a barrier film one by one using a mask for storage electrode formation, and is electrically connected with a plug, and a stage which forms a conducting film spacer for storage electrodes in each side walls of a barrier film and a conducting film.

[0020]According to this invention for attaining the purpose mentioned above, a semiconductor memory device, A semiconductor substrate, an insulator layer formed on a semiconductor substrate, and a plug which pierced through an insulator layer and was electrically connected with a semiconductor substrate, It is more relatively [including a conducting film spacer formed in each side walls of a plug, a barrier film formed on an insulator layer, a conducting film for storage electrodes formed on a barrier film, and a barrier film and a conducting film / a barrier film / than a conducting film] thick.
[0021]
[Embodiment of the Invention]If drawing 2 (C) and drawing 3 (C) are referred to, a barrier film will be thickly formed on an insulator layer including the plug which was filled up with conductive material in the contact hole and in which a new semiconductor memory device by the embodiment of this invention and a manufacturing method for the same were formed, and the conducting film for storage electrodes will be formed on a barrier film. Under the present circumstances, a conducting film is relatively formed thinly from a barrier film. By etching a conducting film and a barrier film one by one using the mask for storage electrode formation, the storage electrode layer electrically connected with a plug is formed, and the conducting film spacer for storage electrodes is formed in each side walls of a barrier film and a conducting film. Such a semiconductor memory device and a manufacturing method for the same, Side vacuum evaporation of the storage electrode of a transition metal can be minimized at the time of the dry etching for storage electrode formation by forming the conducting film for storage electrodes thinly, and forming thickly relatively from a conducting film for electric capacity reservation of the barrier film improved by etching, The bridge between storage electrodes can be prevented.
[0022]Hereafter, with reference to drawing 2 (A) thru/or drawing 2 (D), a 1st embodiment of this invention is described in detail. Drawing 2 (A) thru/or drawing 2 (D) are the figures showing the process of a semiconductor memory device by a 1st embodiment of this invention, and a manufacturing method for the same one by one. Reference of drawing 2 (A) will form an element isolation film for a semiconductor memory device by the embodiment of this invention and a manufacturing method for the same to define an active region and a non-active region as the semiconductor substrate 100 first (not shown).
[0023]On the semiconductor substrate 100, gate oxide is placed in between and the gate electrode layer 103 is formed. The gate electrode layer 103 is formed so that it may be surrounded with the polysilicon 103a, the silicide 103b, and the insulator layer of as [whose each side walls of the gate electrode in which the silicon nitride film 103c was laminated are the silicon nitride film spacers 103d].
[0024]The oxide film 104 for layer insulation is formed on the semiconductor substrate 100

including the gate electrode layer 103. Bit lines are formed in the oxide film 104 (not shown).
[0025]It is more detailed and the 1st oxide film that has the flat upper surface is formed on the semiconductor substrate 100 including the gate electrode layer 103. After bit lines are formed on the 1st oxide film, the 2nd oxide film that has the flat upper surface is formed on the 1st oxide film including bit lines.
[0026]And the storage electrode contact hole 106 is formed by etching the oxide film 104 until the surface of the semiconductor substrate 100 is exposed using the mask for contact hole formation. After conductive material, for example, polysilicon, was filled up with the contact hole 106, The storage electrode contact plug 107 which is etched evenly and is electrically connected with the semiconductor substrate 100 by any one in CMP (chemical mechanical polishing) and an etchback (etch back) process is formed.
[0027]The 1st barrier film (barrier layer) 108 is formed on the oxide film 104 including the plug 107. the oxide in which the 1st barrier film 108 contains at least one in barium, strontium, and a ruthenium, TiN, TiSiN, TiAlN, TaSiN, TaAlN, ruthenium oxide, and iridium oxide -- and, It is formed by any one in lanthanum trioxide strontium cobalt.
[0028]The 1st barrier film 108 is a film for preventing oxidation of polysilicon of the substance for plug 107 formation.
[0029]The 1st conducting film 110 for storage electrodes is formed on the 1st barrier film 108. The 1st conducting film 110 is formed by any one in the substance, for example, TiN, which is comparatively easy to etch, the polysilicon (polysilicon), and a ruthenium. The 1st conducting film 110 is formed in [thickness] 1000A thru/or 10000 A.
[0030]Then, the 2nd barrier film 112 is formed on the 1st conducting film 110. the oxide in which the 2nd barrier film 112 contains at least one in barium, strontium, and a ruthenium, TiN, TiSiN, TiAlN, TaSiN, TaAlN, ruthenium oxide, and iridium oxide -- and, It is formed by any one in lanthanum trioxide strontium cobalt. The 2nd barrier 112 is formed in [thickness] 100A thru/or 1000 A.
[0031]The 2nd conducting film 114 for storage electrodes is formed on the 2nd barrier film 112. The 2nd conducting film 114 is formed in [thickness] 100A thru/or 1000 A relatively more thinly than the 1st conducting film 110.
[0032]The 2nd conducting film 114 is formed by any one in barium, strontium, the oxide that contains at least one in a ruthenium, a ruthenium and platinum, iridium, iridium oxide, ruthenium oxide, and lanthanum trioxide strontium cobalt.
[0033]The 2nd conducting film 114 remains in part also after a following process, and plays a capacitor lower part electrode role. And the 2nd barrier film 112 is a film for preventing the 1st conducting film 110 from oxidizing by a reaction with the 2nd conducting film 114.
[0034]After that, the mask 116 is formed on the 2nd conducting film 114. The mask 116 is formed in [thickness] 500A thru/or 5000 A.
[0035]In drawing 2 (B), after patterning the mask 116 using a photoresist film pattern, a photoresist film pattern is removed (not shown). A photoresist film pattern is formed by any one in monolayer photoresist (single layer resist:SLR) or multilayer photoresist (multi layer resist:MLR). SLR comprises one layer of photoresist and MLR comprises lower photoresist, an oxide film, and top photoresist. As for MLR, it is advantageous to form narrowly an interval with the pattern of the cell by which high integration was carried out.
[0036]The storage electrode layer electrically connected with the plug 107 is formed by etching the 2nd conducting film 114, the 2nd barrier film 112, the 1st conducting film 110, and the 1st barrier film 108 one by one using the patternized mask 116.

[0037]The mask 116 is etched when etching the conducting film 110,114 and the barrier film 108,112. A photoresist film pattern and the mask 116 are etched by any one in RIE (reactive ion etching) of dry etching equipment, and RIBE (reactive ion beam etching).
[0038]The mask 116 has the structure where the oxide film was laminated on Ti or a TiN film, and the 2nd conducting film 114, the 2nd barrier film 112, the 1st conducting film 110, and the 1st barrier film 108 which were laminated by the lower part using this are etched. Here the oxide film of the mask 116 Ti or a TiN film, It is exhausted thoroughly, playing the mask role which etches the 2nd conducting film 114, the 2nd barrier film 112, and the 1st conducting film 110 one by one, and Ti or a TiN film is exhausted thoroughly after that, playing the mask role which etches the 1st barrier film 108.
[0039]Under the present circumstances, the step coverage (stepcoverage) of a high dielectric film is raised by a following process by etching so that the grade of a section may maintain 80 degrees - 90 " at the time of etching of the 2nd conducting film 114, the 2nd barrier film 112, the 1st conducting film 110, and the 1st barrier film 108.
[0040]Reference of drawing 2 (B) will form the 3rd barrier film 118 so that the oxide film 104 may be thoroughly covered including the 2nd conducting film 114. The 3rd barrier film 118 is vapor-deposited by any one in the sputtering (sputtering) method and the CVD (chemical vapor deposition) method.
[0041]By the step part of a storage electrode, since step coverage is bad, a sputtering method inclines at 80 degrees - about 90 degrees, and inclination in the 1st, the 2nd, the 3rd, and the section of the 4th conducting film must be vapor-deposited uniformly. On the other hand, since a CVD method is vapor-deposited by stranski-krastinove mode, it is excellent without a relation in step coverage to inclination in a section. Therefore, it is satisfactory even if the section of the conducting film which comprised a composite layer becomes almost vertical, when vapor-depositing with a CVD method.
[0042]the 3rd barrier film 118 -- the 1st and 2nd barrier films 108,112 -- the same -- barium and strontium -- and, It is formed by any one in the oxide which contains any one in a ruthenium, TiN, TiSiN, TiAlN, TaSiN, TaAlN, ruthenium oxide, iridium oxide, and lanthanum trioxide strontium cobalt. The 3rd barrier film 118 is formed in [thickness] 100A thru/or 1000 A.
[0043]In drawing 2 (C), the barrier-metal spacer 118a is formed in each side walls of the 2nd conducting film 114, the 2nd barrier film 112, the 1st conducting film 110, and the 1st barrier film 108 by etching the 3rd barrier film 118 by an etch back process until the surface of the 2nd conducting film 114 is exposed.
[0044]Then, the 3rd conducting film 120 is formed on the oxide film 104 including the barrier-metal spacer 118a and the 2nd conducting film 114. The 3rd conducting film 120 is formed by any one in barium, strontium, the oxide that contains any one in a ruthenium, a ruthenium and platinum, iridium, iridium oxide, ruthenium oxide, and lanthanum trioxide strontium cobalt.
[0045]The conducting film spacer 120a is formed in each side walls of the barrier-metal spacer 118a by etching the 3rd conducting film 120 by an etch back process. Therefore, the storage electrode of a capacitor lower part electrode is formed.
[0046]Here, the barrier-metal spacer 118a is used as a film for inhibiting the reaction of the silicon of the oxygen which pierces through the conducting film spacer 120a at the time of vacuum evaporation of a capacitor dielectric film, for example, a BST oxide film, and enters on the conducting film spacer 120a, and the 1st conducting film 110.
[0047]Reference of drawing 2 (D) will form the capacitor dielectric film 122 on the oxide film 104 including a storage electrode. The capacitor dielectric film 122 is formed by any one in

barium titanate strontium and strontium titanate. The capacitor dielectric film 122 is formed in [thickness] 200A thru/or 1000 A, and is vapor-deposited by any one in a sputtering method or a CVD method.
[0048]The capacitor upper electrode 124 is formed on the capacitor dielectric film 122. The number of the capacitor upper electrodes 124 is any one in platinum, iridium, and a ruthenium, and they are formed in [thickness] 100A thru/or 2000 A. The upper electrode 124 is vapor-deposited by any one in a sputtering method or a CVD method. Therefore, a high dielectric capacitor is formed.
[0049]Here, the 1st, the 2nd, and the 3rd barrier film 108,112,118 are used also not only as a barrier role but as a storage electrode.
[0050]The 2nd conducting film 114 formed on the 2nd barrier film 112 is relatively thinner than the 1st conducting film 110.
[0051]Drawing 3 (A) thru/or drawing 3 (D) are the figures showing the process of a semiconductor memory device by a 2nd embodiment of this invention, and a manufacturing method for the same one by one. Since it seems that the process of etching an insulator layer and forming the contact hole 206, and it being filled up with conductive material and forming the plug 207 described by a 1st embodiment, it carries out abbreviated. Reference of drawing 3 (A) will form the barrier film 208 on the oxide film 204 including the plug 207 first. the oxide in which the barrier film 208 contains at least one in barium, strontium, and a ruthenium, TiN, TiSiN, TiAlN, TaSiN, TaAlN, ruthenium oxide, and iridium oxide -- and, It is formed by any one in lanthanum trioxide strontium cobalt, and the former is thickly formed comparatively relatively in [thickness] 1000A thru/or 10000 A.
[0052]Then, the 1st conducting film 210 for storage electrodes is formed on the barrier film 208. The 1st conducting film 210 is formed by any one in barium, strontium, the oxide that contains any one in a ruthenium, a ruthenium and platinum, iridium, iridium oxide, ruthenium oxide, and lanthanum trioxide strontium cobalt.As for the 1st conducting film 210, the former is formed comparatively thinly in [thickness] 300A thru/or 2000 A.
[0053]Therefore, the thickness of the barrier film 208 is formed more thickly about 3 or more times than the thickness of the 1st conducting film 210. Also after a succession etching process, the 1st conducting film 210 remains in part, and is used as a lower electrode.
[0054]Here, the barrier film 208 is a film for preventing oxidation of polysilicon of the substance for plug 207 formation.
[0055]The mask 212 is formed on the 1st conducting film 210. The mask 212 is patterned using a photoresist film pattern as a mask. The number of photoresist film patterns is any one in monolayer photoresist SLR and the multilayer photoresist MLR.
[0056]The storage electrode layer electrically connected with the plug 207 is formed by etching the 1st conducting film 210 and the barrier film 208 one by one until the surface of the oxide film 204 is exposed using the patterned mask 212.
[0057]The mask 212 is etched at the time of etching of the 1st conducting film 210 and the barrier film 208. The mask 212 and a photoresist film pattern are etched by any one dry etching equipment in RIE or RIBE. The mask 212 is that the 1st conducting film 210 that has the structure where the oxide film was laminated on Ti or a TiN film, and was laminated by the lower part using this, and the barrier film 208 are etched.
[0058]Here, the oxide film of the mask 212 is exhausted thoroughly, being used as a mask which etches Ti or a TiN film, and the 1st conducting film 210 one by one, and Ti or a TiN film is exhausted thoroughly after that, playing the mask role which etches the barrier film 208 of a

barrier film. When etching the 1st conducting film 210 and the barrier film 208, the step coverage of a high dielectric film is made to increase by a following process, when the grade of a section maintains 80 degrees - 90 ".
[0059]The 2nd conducting film 214 for storage electrodes is formed on the oxide film 204 including the 1st conducting film 210. The 2nd conducting film 214 is vapor-deposited by any one in a sputtering method and a CVD method, and is formed in [thickness] 500A thru/or 1000 A. When vapor-depositing with a sputtering method, 80 degrees - about 90 degrees must incline inclination in the section of the barrier film 208 and the 1st conducting film 210, and uniform vacuum evaporation must become, and when vapor-depositing with a CVD method, it is satisfactory even if the section of the barrier film 208 and the 1st conducting film 210 becomes almost vertical.
[0060]Although dry etching is identically [to the 1st conducting film 210] difficult for the 2nd conducting film 214 (drawing 3 (B)), the platinum which has the excellent characteristic with the lower electrode of a BST capacitor dielectric film, iridium, iridium oxide, ruthenium oxide, lanthanum trioxide strontium cobalt, and a ruthenium -- and, It is formed by any one in the oxide which contains any one in barium, strontium, and a ruthenium. And the 2nd conducting film 214 is used also as a barrier film for a BST capacitor dielectric film to prevent the barrier film 208 from oxidizing.
[0061]The storage electrode of a capacitor lower part electrode is formed by carrying out overall etching of the 2nd conducting film 214 without a mask by an etch back process, and forming the conducting film spacer 214a (drawing 3 (C)) in each side walls of the barrier film 208 and the 1st conducting film 210.
[0062]The capacitor dielectric film 216 (drawing 3 (D)) is formed on the oxide film 204 including a storage electrode. The capacitor dielectric film 216 is formed with any one high dielectric film in barium titanate strontium and strontium titanate, and has the thickness range of 200A thru/or 1000 A. The capacitor dielectric film 216 is vapor-deposited with a sputtering method or a CVD method.
[0063]Finally, a capacitor is formed by forming the upper electrode 218 on the capacitor dielectric film 216. The number of upper electrode 218 substances is any one in platinum, iridium, and a ruthenium, and they are formed in [thickness] 100A thru/or 2000 A. The upper electrode 218 is vapor-deposited by any one in a sputtering method or a CVD method.
[0064]The barrier film 208 formed on the plug 207 and the insulator layer 204 is relatively thicker than the conducting film 210 for storage electrodes formed on the barrier film 208.
[0065]Platinum in which storage electrode structure which was mentioned above is excellent at the lower electrode of a BST capacitor dielectric film, It is tinged with the gestalt which wraps a barrier film thoroughly, and at the time of a BST oxide film or a succession heat treatment process, as soon as they have a capacitor lower electrode characteristic which prevents oxidation of polysilicon by oxygen, electrodes, such as iridium and a ruthenium, reduce the number of times of electrode vacuum evaporation considering a 1st embodiment, and they are advantageous to it at the time of mass production application.
[0066]Since a spacer process is added only once, in the space margin between lower electrodes, it is more advantageous than the storage electrode structure of a 1st embodiment. spreading the thickness of the barrier film furthermore improved by etching -- a storage electrode -- public funds -- using it as a group film -- super-high integration -- it is dynamic and is the structure where the electric capacity of the capacitor demanded is securable.
[0067]

[Effect of the Invention]Storage electrode side vacuum evaporation of a transition metal can be minimized at the time of the dry etching for storage electrode formation by this invention's forming the conducting film for storage electrodes thinly, and forming thickly relatively from a conducting film for electric capacity reservation of the barrier film improved by etching, There is an effect which the bridge between storage electrodes can prevent.

CLAIMS

[Claim(s)]
[Claim 1]A manufacturing method of a semiconductor memory device characterized by comprising the following.
A stage which forms an insulator layer on a semiconductor substrate on which a transistor was accumulated.
A stage which etches said insulator layer and forms a storage electrode contact hole until the surface of said semiconductor substrate is exposed using a mask for contact hole formation.
A stage which forms a storage electrode contact plug which fills up said contact hole with conductive material, and is electrically connected with a semiconductor substrate.
said plug is included -- said insulator layer top -- the 1st barrier film and the 1st conducting film -- and, A stage which forms the 2nd barrier film one by one, and a stage which forms the 2nd conducting film for storage electrodes on said 2nd barrier film, and forms said 2nd conducting film thinly relatively from said 1st conducting film, using a mask for storage electrode formation -- said 2nd conducting film, the 2nd barrier film, and the 1st conducting film -- and, A stage which forms a storage electrode layer which etches the 1st barrier film one by one, and is electrically connected with said plug, A stage which forms a barrier-metal spacer in each side walls of said 2nd conducting film, the 2nd barrier film, the 1st conducting film, and the 1st barrier film, and a stage which forms a conducting film spacer for storage electrodes in each side walls of said barrier-metal spacer.

[Claim 2]said 1st barrier film, the 2nd barrier film, and a barrier-metal spacer -- barium and strontium -- and, an oxide which contains any at least one in a ruthenium, TiN, TiSiN, TiAlN, TaSiN, TaAlN, ruthenium oxide, and iridium oxide -- and, A manufacturing method of the semiconductor memory device according to claim 1 forming by any one in lanthanum trioxide strontium cobalt.
[Claim 3]A manufacturing method of the semiconductor memory device according to claim 1, wherein said 2nd barrier film and a barrier-metal spacer are formed in [thickness] 100A thru/or 1000 A.
[Claim 4]A manufacturing method of the semiconductor memory device according to claim 1, wherein said 1st conducting film is formed by any one in TiN, polysilicon, and a ruthenium.
[Claim 5]A manufacturing method of the semiconductor memory device according to claim 1, wherein said 1st conducting film is formed in [thickness] 1000A thru/or 10000 A.
[Claim 6]an oxide in which said 2nd conducting film and a conducting film spacer contain any at least one in barium, strontium, and a ruthenium, a ruthenium and platinum, iridium, iridium oxide, and ruthenium oxide -- and, A manufacturing method of the semiconductor memory device according to claim 1 forming by any one in lanthanum trioxide strontium cobalt.
[Claim 7]A manufacturing method of the semiconductor memory device according to claim 1, wherein said 2nd conducting film is formed in [thickness] 100A thru/or 1000 A.

[Claim 8]A semiconductor memory device comprising:
A semiconductor substrate.
An insulator layer formed on said semiconductor substrate.
A plug which pierced through said insulator layer and was electrically connected with said semiconductor substrate.
Said plug, the 1st barrier film formed on an insulator layer, and the 1st conducting film for storage electrodes formed on said 1st barrier film, A barrier-metal spacer formed in each side walls of the 2nd barrier film formed on said 1st conducting film, the 2nd conducting film thinly formed on said 2nd barrier film, said 2nd conducting film and the 2nd barrier film, the 1st conducting film, and the 1st barrier film, and a conducting film spacer formed in each side walls of said barrier-metal spacer.

[Claim 9]A stage which forms an insulator layer on a semiconductor substrate on which a transistor was accumulated, A stage which etches said insulator layer and forms a contact hole until the surface of said semiconductor substrate is exposed using a mask for contact hole formation, A stage which forms a plug which fills up said contact hole with conductive material, and is electrically connected with said semiconductor substrate, A stage which forms a barrier film thickly on said insulator layer including said plug, and a stage which forms a conducting film for storage electrodes on said barrier film, and forms said conducting film thinly relatively from a barrier film, A stage which forms a storage electrode layer which etches said conducting film and a barrier film one by one using a mask for storage electrode formation, and is electrically connected with said plug, A manufacturing method of a semiconductor memory device including a stage which forms a conducting film spacer for storage electrodes in each side walls of said barrier film and a conducting film.
[Claim 10]an oxide in which said barrier film contains at least one in barium, strontium, and a ruthenium, TiN, TiSiN, TiAlN, TaSiN, TaAlN, ruthenium oxide, and iridium oxide -- and, A manufacturing method of the semiconductor memory device according to claim 9 forming by any one in lanthanum trioxide strontium cobalt.
[Claim 11]an oxide in which said conducting film and a storage electrode spacer contain any at least one in barium, strontium, and a ruthenium, a ruthenium and platinum, iridium, iridium oxide, and ruthenium oxide -- and, A manufacturing method of the semiconductor memory device according to claim 9 forming by any one in lanthanum trioxide strontium cobalt.
[Claim 12]A manufacturing method of the semiconductor memory device according to claim 9, wherein said barrier film is formed in [thickness] 1000A thru/or 10000 A and said conducting film for storage electrodes is formed in [thickness] 300A thru/or 2000 A.
[Claim 13]A manufacturing method of the semiconductor memory device according to claim 12, wherein thickness of said conducting film forms thickness of said barrier film thickly 3 or more times comparatively.
[Claim 14]A manufacturing method of the semiconductor memory device according to claim 9, wherein said storage electrode spacer is formed in [thickness] 500A thru/or 1000 A.
[Claim 15]A semiconductor substrate, an insulator layer formed on said semiconductor substrate, and a plug which pierced through said insulator layer and was electrically connected with said semiconductor substrate, A semiconductor memory device characterized by said barrier film being relatively thicker than said conducting film including a conducting film spacer formed in each side walls of said plug, a barrier film formed on an insulator layer, a conducting film for storage electrodes formed on said barrier film, and said barrier film and a conducting film.

[Translation done.]